ABSTRACT OF THE DISCLOSURE

An image suppression filter circuit comprises a first phase shifter outputting a first output signal and a second output signal substantially orthogonal thereto, a second phase shifter outputting a third output signal and a fourth output signal orthogonal to the third output signal, a first subtracter subtracting the fourth output signal from the first output signal, a first adder adding the second and third output signals, a third phase shifter outputting a fifth output signal and a sixth output signal orthogonal to the fifth output signal, a fourth phase shifter outputting a seventh output signal and an eighth output signal orthogonal thereto, a second subtracter subtracting the eighth output signal from the fifth output signal, and a second adder adding the sixth and the seventh output signals.